

IN THE CLAIMS:

Claim 1 is amended herein. Claims 2-19 are added. All pending claims and their present status are reproduced below.

1 1. (Currently amended) A multithreaded computer based system for enabling
2 a command in a first thread to access~~[[ing]]~~ data in a second thread comprising:
3 an embedded pipelined processor capable of having a first program thread and a
4 second program thread in an execution pipeline, said first program thread
5 comprising a first set of instructions, said second program thread
6 comprising a second set of instructions, said embedded processor
7 comprising:
8 a fetch unit for fetching an instruction from program memory;
9 a decode unit for decoding said fetched ~~[[feteched]]~~ instruction;
10 an execution unit for executing said decoded instruction~~[[s]]~~; and
11 a write back unit for writing the results of said executed instruction to an
12 identified storage location;
13 a first set of data storage devices capable of storing a first state of said embedded
14 processor, wherein said first state is the state of the embedded processor
15 during the execution of the first program thread~~[[, including]]~~
16 ~~a first control status register for identifying a first target set of data storage~~
17 ~~devices from which a first source operand of a first fetched~~
18 ~~instruction is to be retrieved from and for identifying a second~~
19 ~~target set of data storage devices to which a first result of a first~~
20 ~~executed instruction is stored, wherein said first and second target~~
21 ~~set of data storage devices are different;~~

22 a second set of data storage devices capable of storing a second state of said
23 embedded processor, wherein said second state is the state of the
24 embedded processor during the execution of the second program thread[[,
25 including:]]
26 ~~a second control status register for identifying a third target set of data~~
27 ~~storage devices from which a second source operand of a second~~
28 ~~fetch instruction is to be retrieved from and for identifying a~~
29 ~~fourth target set of data storage devices to which a second result of~~
30 ~~a second executed instruction is stored, wherein said third and~~
31 ~~fourth target set of data storage devices are different;~~
32 wherein at least said first set of data storage devices includes a control status
33 register for identifying a first target set of data storage devices from which
34 a first source operand of a fetched instruction is to be retrieved and for
35 identifying a second target set of data storage devices to which a first
36 result of an executed instruction is to be stored, wherein at least one of
37 said first or said second target set of data storage devices is included in the
38 second set of data storage devices;
39 a thread scheduler for identifying which of said program threads said embedded
40 processor executes; and
41 an instruction set including an instruction that overwrites the first control status
42 register when instructions associated with the first set of data storage
43 devices are executed and overwrites the second control status register

44 when instructions associated with the second set of data storage devices
45 are executed;
46 wherein said processor switches between said first and second state in a time
47 period between the end of the execution of a first program instruction in the first thread
48 and the beginning of the execution of a second program instruction in the second thread;
49 wherein said processor switches between said first and second states by changing
50 a state selection register.

1 2. (New) The multithreaded computer based system of claim 1, wherein the
2 embedded pipelined processor further includes a peripheral block.

1 3. (New) The multithreaded computer based system of claim 2, wherein the
2 peripheral block is one of a phase locked loop and a watchdog timer.

1 4. (New) The multithreaded computer based system of claim 1, wherein the
2 embedded pipelined processor further includes an internal memory unit comprising a
3 flash memory with a shadow static memory.

1 5. (New) A method of executing instructions in a multithread computer based
2 system having at least a first thread associated with a first context including a set of
3 context registers, the method comprising the steps of:
4 selecting the first thread associated with the first context;
5 fetching a first instruction of the first thread which indicates source data registers
6 associated with operands, each operand associated with a context
7 comprising data registers;

8 decoding the instruction to determine the context and the source data register
9 associated with a first operand;
10 executing the instruction on the first operand to produce a result; and
11 storing the result in a destination data register.

1 6. (New) The method of claim 5, wherein the decoding further comprises decoding
2 the instruction to determine the context and the source data register associated with a
3 second operand, the context associated with the first operand being the first context and
4 the context associated with the second operand being a second context different from the
5 first context.

1 7. (New) The method of claim 5, wherein the destination data register is part of a
2 second set of context registers of a second thread different from the first thread.

1 8. (New) The method of claim 7, wherein the decoding step further comprises
2 determining a context of the destination data register for storing the result.

1 9. (New) The method of claim 5, wherein the executing includes modifying a
2 control and status register to indicate the context of the first operand being different than
3 the first context.

1 10. (New) The method of claim 9, wherein the executing further includes modifying
2 the control and status register to indicate a context of the destination data register being
3 different than the first context.

1 11. (New) An apparatus for executing instructions in a multithread computer based
2 system having at least a first thread associated with a first context comprising a set of
3 context registers, the apparatus comprising:

4 means for selecting the first thread associated with the first context;

5 means for fetching a first instruction of the first thread which indicates source
6 data registers associated with operands, each operand associated with a
7 context comprising data registers;

8 means for decoding the instruction to determine the context and the source data
9 register associated with a first operand;

10 means for executing the instruction on the first operand to produce a result; and

11 means for storing the result in a destination data register.

1 12. (New) A multithread embedded processing system wherein cross-thread access is
2 enabled between multiple pipelined threads, the system comprising a processor and a
3 control and status register, the control and status register having:

4 a set of source thread selection bits for indicating to the processor a source context
5 of a source thread from which source operands are obtained to be used in a
6 currently executed thread; and

7 a set of destination thread selection bits for indicating to the processor a
8 destination context of a destination thread to which execution results of
9 the currently executed thread are written.

1 13. (New) The multithread embedded processing system of claim 12, wherein the
2 control and status register further comprises an enable source override bit for the

processor to select between the context of the currently executed thread and the source context indicated in the source thread selection bits.

14. (New) The multithread embedded processing system of claim 12, wherein the control and status register further comprises an enable destination override bit for the processor to select between the context of the currently executed thread and the destination context indicated in the destination thread selection bits.

15. (New) The multithread embedded processing system of claim 12, wherein the multiple pipelined threads comprise:

a hardware thread having a context, the hardware thread communicatively coupled to hardware inputs and outputs for executing tasks; and
a supervisory thread for controlling the multiple pipelined threads using the control and status register, wherein the controlling occurs one thread at a time and includes suspending the one thread, reading the one thread's state, saving the one thread's state, modifying the one thread's state by writing to the one thread's context, and resuming the one thread, thereby changing the tasks being executed in the one thread.

16. (New) The multithread embedded processing system of claim 12, wherein the control and status register is modified by executing a set control and status register instruction that enables a second thread to overwrite the contents of the control and status register of the currently executed thread.

17. (New) The multithread embedded processing system of claim 12, further comprising a plurality of registers shared by the multiple pipelined threads.

1 18. (New) The multithread embedded processing system of claim 12, wherein each
2 pipelined thread has an associated set of context registers for storing the thread's state,
3 each set of context registers comprising:

4 a set of general-purpose registers coupled to the processor for executing
5 instructions;

6 a set of address registers coupled to the processor for functioning as pointers to
7 memory locations;

8 a stack pointer register coupled to the processor for storing a stack offset;

9 a high multiple-accumulate result storage register (MAC_HI) coupled to the
10 processor for storing a first set of bits of a multiple-accumulate result;

11 a low multiple-accumulate result storage register (MAC_LO) coupled to the
12 processor for storing a second set of bits of the multiple-accumulate result;

13 a rounded and clipped multiple accumulate result storage register (MAC_RC16)
14 coupled to the processor for creating a digital signal of lower precision
15 than a signal provided by the MAC_HI and MAC_LO registers;

16 a source register coupled to the processor for providing an additional operand in
17 instructions requiring more than 2 operands; and

18 a context counter register coupled to the processor for maintaining a count of
19 executed instructions in the thread with which the context is associated.

1 19. (New) The multithread embedded processing system of claim 18, wherein each
2 register is a 32 bit register.